KLAS H. EKLUND

041994
2 OF 2
250
SS-520-01

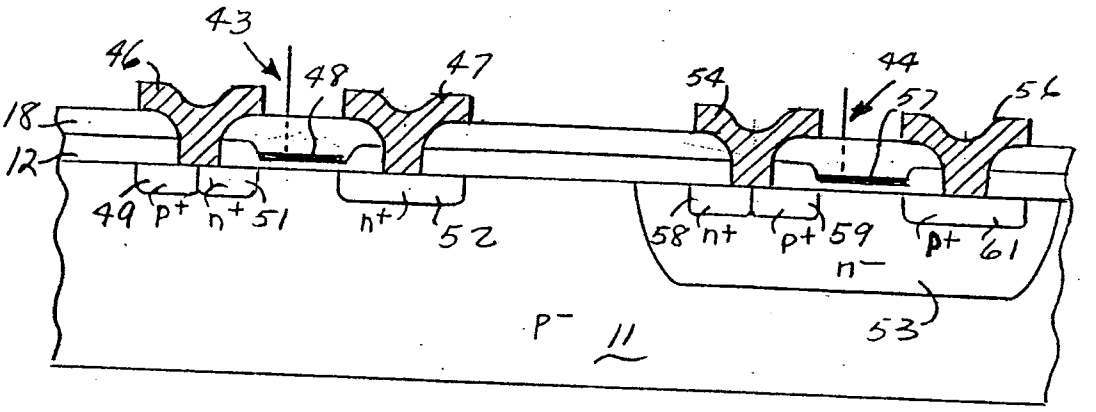

Fig-4

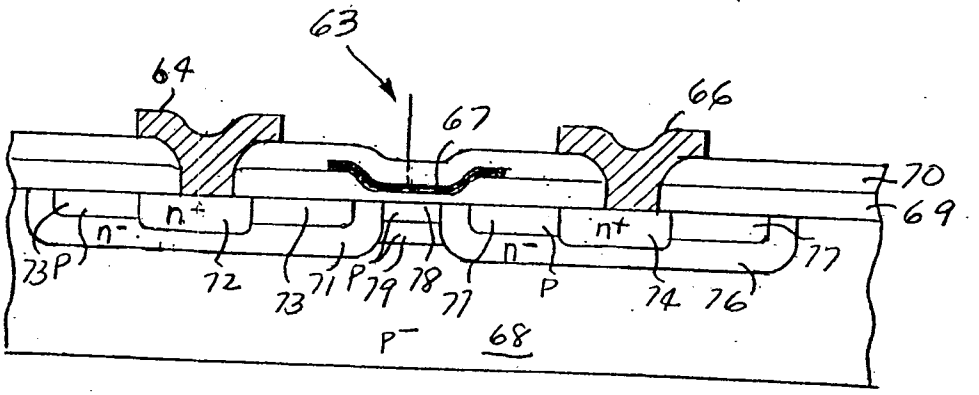

Fig_5

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
07/041,994	04/24/87	ERLUND K	013-320-01

THOMAS E. SCHATZEL
3211 SCOTT BLVD., STE. 201
SANTA CLARA, CA 95054-3093

EXAMINER	
JACKSON, J.	
ART UNIT	PAPER NUMBER
253	2

DATE MAILED: 12/07/87

This is a communication from the examiner in charge of your application.

COMMISSIONER OF PATENTS AND TRADEMARKS

☐ This application has been examined ☐ Responsive to communication filed on _____ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), — days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☒ Notice re Patent Drawing, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449
4. ☐ Notice of Informal Patent Application, Form PTO-152
5. ☐ Information on How to Effect Drawing Changes, PTO-1474
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☒ Claims 1-18 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 1-18 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings which are acceptable for examination purposes until such time as allowable subject matter is indicated.
8. ☐ Allowable subject matter having been indicated, formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. These drawings are ☐ acceptable; ☐ not acceptable (see explanation).
10. ☐ The ☐ proposed drawing correction and/or the ☐ proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved. ☐ disapproved (see explanation). However, the Patent and Trademark Office no longer makes drawing changes. It is now applicant's responsibility to ensure that the drawings are corrected. Corrections MUST be effected in accordance with the instructions set forth on the attached letter "INFORMATION ON HOW TO EFFECT DRAWING CHANGES", PTO-1474.
12. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

PTOL-326 (Rev. 7-82) EXAMINER'S ACTION

On page 9 line 28 "72" should be --73--.

Claims 1, 2, 4-7, 16 are rejected under 35 U.S.C. 112, first and second paragraphs, as the claimed invention is not described in such full, clear, concise and exact terms as to enable any person skilled in the art to make and use the same, and/or for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The structure of claim 1 is indefinite. The language "being united in one structure" is vague and indefinite and does not clearly or concretely define the structure of applicant's invention. The terms "insulated gate FET" and "double sided JFET" are also broad and do not define applicant's invention. Claim 2 is confusing since lines 14-17 mimic lines 17-20. The other claims are rejected for dependence on 1 or 2.

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP 608.01(o). Correction of the following is required: there is no proper antecedent in the specification for the process descriptions of claims 11, 13, 14, 17.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless-

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international

application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-3, 5-9, 11, 12, 16 rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103 as obvious over Colak.

Colak shows a DMOS device wherein layer 16 may perform the function of a JFET gate "on top of" an extended drain region 14 in the embodiment of figs. 2B or 2C. Substrate layer 12 may act as the other gate of the JFET. Clearly claim 1 does not distinguish over Colak. Note that mere labels as "JFET" do not structurally distinguish the claims over Colak since the structure of Colak may be labeled an IGFET in series with a double sided JFET as shown above. Claim 2 also does not distinguish over Colak since the claimed structure is shown in Colak and the intended use language "whereby current flow..." in claim 2 does not structurally distinguish over Colak and furthermore Colak's device may perform the same intended function. See In re Pearson 181 USPQ 642 or Ex parte Minks 169 USPQ 120 on statements of intended use in claims drawn to structure as we have here. Similarly claim 3 does not distinguish over Colak. Claim 5 is a product by process claim which does not structurally distinguish applicant's final product over Colak.

A "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re

Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by Process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear.

Claim 6 also is undistinguishing over Colak since the thickness of layer 16 is a design variable and 1 micron thickness would not be unobvious to one of ordinary skill in view of Colak. Similarly, in re claim 7 a dopant density of greater than $5x10^{16}$/cc would not be unobvious for the doping density of layer 16 of Colak. Claims 8, 9 also are obvious over Colak. Claims 11, 12 are product by process claims which also do not distinguish the final product over Colak. Claim 16 also does not distinguish over Colak as "floating" is vague and undistinguishing.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at

the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Claims 4, 10, 13-15, 17 and 18 rejected under 35 U.S.C. 103 as being unpatentable over Colak in view of Thomas.

Thomas shows the obvious of providing low voltage and high voltage devices on the same substrate. It would be obvious from Thomas to practice Colak as CMOS or with other devices. Claim 4 is hence obvious. In re claims 10, 13, 15 "well" regions are also obvious from Thomas. Claims 14, 17 also are product by process claims which do not distinguish the final product over the suggestions of the references on final structure. Claim 18 also does not distinguish over the suggestions of Colak in view of Thomas.

Any inquiry concerning this communication should be directed to J. Jackson at telephone number 703-557-4824.

Jackson/EW
12-2-87

ANDREW J. JAMES
SUPERVISORY PATENT EXAMINER
GROUP ART UNIT 253

PTO - 948 (Rev. 8-82)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

ATTACHMENT TO PAPER NUMBER 2

GROUP 260

S.N. 41994

NOTICE OF PATENT DRAWINGS OBJECTION

Drawing Corrections and/or new drawings may only be submitted in the manner set forth in the attached letter, "Information on How to Effect Drawing Changes" PTO-1474.

A. ☒ The drawings, filed on 4/24/89, are objected to as informal for reason(s) checked below:

1. ☐ Lines Pale.
2. ☐ Paper Poor.
3. ☒ Numerals Poor.
4. ☒ Lines Rough and Blurred. FIGS 1-5
5. ☐ Shade Lines Required.
6. ☐ Figures Must be Numbered.
7. ☐ Heading Space Required.
8. ☐ Figures Must Not be Connected.
9. ☐ Criss-Cross Hatching Objectionable.
10. ☐ Double-Line Hatching Objectionable.
11. ☐ Parts in Section Must Be Hatched.
12. ☐ Solid Black Objectionable.
13. ☐ Figure Legends Placed Incorrectly.
14. ☐ Mounted Photographs.
15. ☒ Extraneous Matter Objectionable. [37 CFR 1.84 (1)] BORDER LINES
16. ☐ Paper Undersized; either 8½" x 14", or 21.0 cm. x 29.7 cm. required.
17. ☐ Proper A4 Margins Required:
    ☐ TOP 2.5 cm. ☐ RIGHT 1.5 cm.
    ☐ LEFT 2.5 cm. ☐ BOTTOM 1.0 cm.
18. ☐ Other:

B. ☒ The drawings, submitted on 4/24/89, are so informal they cannot be corrected. New drawings are required. Submission of the new drawings MUST be made in accordance with the attached letter.

TO SEPARATE, HOLD TOP AND BOTTOM EDGES, SNAP–APART AND DISCARD CARBON

FORM PTO-892 (REV. 3-78) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

NOTICE OF REFERENCES CITED

SERIAL NO.	GROUP ART UNIT	ATTACHMENT TO PAPER NUMBER
041994	253	2

APPLICANT(S): Eklund

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	A	4626879	12/86	Colak	357	23.8	12/82
	B	4628341	12/86	Thomas	357	23.8	9/85
	C						
	D						
	E						
	F						
	G						
	H						
	I						
	J						
	K						

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG	PERTINENT PP. SPEC.
	L								
	M								
	N								
	O								
	P								
	Q								

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

R	
S	
T	
U	

EXAMINER	DATE
J. Jackson	11/87

* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05 (a).)

#75.00 - 216 - #253

PATENT

Case Docket No. SS-520-01

Date April 7, 1988

In re application of: Klas H. Eklund

Serial No.: 07/041,994

Filed: April 24, 1987

For: HIGH VOLTAGE MOS TRANSISTORS

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

Sir:

Transmitted herewith is an Amendment in the above-identified application.

[ ] No additional fee is required.

[X] Two Month Extension Fee Enclosed. ($85.00)

[ ] Additional fee calculated as follows:

CLAIMS AS AMENDED						
	Claims remaining after amendment		Highest number previously paid for	Present extra	Rate	Addtnl. Fee
Total Claims	_____	Minus	_____ =	_____ x	$12.00	= _____
Indep. Claims	_____	Minus	_____ =	_____ x	$34.00	= _____

Additional Fee Due $ _____

[X] A verified statement claiming small entity status [X] has been filed; _____ is attached. The fee due is fifty percentum of the above.

Fee Due $ _____

[X] A check in the amount of $ 85.00 is attached. (Two Month Extension Fee)

[X] Any additional fees may be charged to Deposit Account No. 19-0310. A duplicate of this transmittal is attached.

Respectfully submitted,

040 04/13/88 041994

By 1 215 85.00 CK
Attorney For Applicant
Reg. No.: 22,617

Law Offices of THOMAS E. SCHATZEL
A Professional Corporation
3211 Scott Boulevard Suite 201
Santa Clara, CA 95054
(408) 727-7077

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on 4-7-88 (Date of Deposit)

Thomas E. Schatzel
Name of Applicant, assignee or Registered Rep.

Signature 4/7/88 Date

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Klas H. Eklund

Serial No.: 07/041,994

Filed : 04-24-87

For : HIGH VOLTAGE MOS TRANSISTORS

Group Art Unit: 253

Examiner: J. Jackson

Attorneys Docket No.: SS-520-01

COMMISSIONER OF PATENTS
& TRADEMARKS
Washington, D.C. 20231

Date of this Paper:
April 7, 1988

AMENDMENT

In response to the U.S. Patent Office Action mailed December 7, 1987 (Paper No. 2), please amend this application as follows:

In the Specification

Page 1, line 26, change "of" to --on--;

Page 9, line 15, insert the following paragraph:

--It should be noted that the term "substrate" refers to the physical material on which a microcircuit is fabricated. If a transistor is fabricated on a well of n or p type material within a primary substrate of opposite type material, the well material can be considered a secondary substrate. Similarly, if a transistor is fabricated on an epitaxial layer or epi-island that merely supports and insulates the transistor, the epitaxial layer or epi-island can be considered a secondary substrate. An epi-island is a portion of an epitaxial layer of one conductivity type that is isolated from the remaining portion of the epitaxial layer by diffusion pockets of an opposite conductivity type. When complimentary transistors are formed on the same chip, the well in which one complimentary transistor is embedded is formed by the same diffusion as the extended drain region for the other transistor.--.

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(Date of Deposit)

Thomas E. Schatzel
Name of Applicant, assignee, or Registered Rep.

Signature 4/7/88
Date

Page 9, line 28, change "72" to --73--.

In the Claims

Cancel claims 1-5 and 8-18.

Add new claims 19-23 as follows:

19. A high voltage MOS transistor comprising:

a semiconductor substrate of a first conductivity type having a surface,

a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,

a source contact connected to one pocket,

a drain contact connected to the other pocket,

an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions,

a surface adjoining layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions,

said top layer of material and said substrate being subject to application of a reverse-bias voltage,

an insulating layer on the surface of the substrate and covering at least that portion between the source contact pocket and the nearest surface-adjoining position of the extended drain region, and

a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the source contact pocket and the nearest surface-adjoining position of the extended drain region, said gate electrode controlling by field-effect the flow of current thereunder through the channel.

20. The high voltage MOS transistor of claim ~~19~~ 1 having one channel conductivity type in combination with a ~~complimentary~~ complementary high voltage MOS transistor of an opposite channel conductivity type combined on the same chip and isolated from each other.

21. The high voltage MOS transistor of claim ~~19~~ 1 combined on the same chip with a low voltage CMOS implemented device.

22. The combination of claim ~~21~~ 5 further including,

a ~~complimentary~~ complementary high voltage MOS transistor, and

a ~~complimentary~~ complementary low voltage CMOS implemented device on the same chip and isolated from each other.

23. A high voltage MOS transistor comprising:

a semiconductor substrate of a first conductivity type having a surface,

a pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface,

a source contact connected to one pocket,

an extended source region of the second conductivity type extending laterally each way from the source contact pocket to a surface-adjoining ~~position~~ positions,

a layer of material of the first conductivity type on top of an intermediate portion of the extended source region between the surface-adjoining positions,

said top layer and said substrate being subject to application of a reverse-bias voltage,

a drain contact connected to the other pocket,

an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions,

a layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions,

said top layer of material and said substrate being subject to application of a reverse-bias voltage,

an insulating layer on the surface of the substrate and covering at least that portion between the nearest surface-adjoining positions of the extended source region and the extended drain region, and

a gate electrode on the insulating layer and electrically isolated from the substrate region thereunder which forms a channel laterally between the nearest surface-adjoining positions of the extended source region and the extended drain region, said gate electrode controlling by field-effect the current flow thereunder through the channel.

Amend the claims as follows:

Claim 6, line 1, change "5" to --19--; and

Claim 7, line 1, change "5" to --19--.

REMARKS

The specification has been amended to correct minor errors and to provide an antecedent basis in the specification for epitaxial layer and epi-island mentioned in former claims 11 and 13.

This invention relates to high voltage, metal oxide semiconductor transistors of the field effect type. There is a need for more efficient transistors which can be made as either discrete or integrated devices of either n-channel or p-channel conductivity. The

integrated devices should be easily combined with low voltage (five volt) control logic on the same chip. Devices of opposite conductivity should be combinable in a complimentary manner on the same chip. Such transistors, with modifications, should be capable of source-follower applications.

The applicant has disclosed a novel and unobvious high voltage MOS transistor having a low threshold voltage that is compatible with five volt control logic and a low ON-resistance. This transistor can be made as either discrete or integrated devices of either n-channel or p-channel conductivity. The high voltage MOS transistors can be modified for source-follower applications by providing both extended source regions and extended drain regions. These transistors are formed on a substrate of a first conductivity type having a surface. A pair of laterally spaced pockets of semiconductor material of a second conductivity type are provided within the substrate and adjoining the substrate surface. A source contact is connected to one pocket and a drain contact is connected to the other pocket. An extended drain region of a second conductivity type extends laterally each way from the drain pocket to surface-adjoining positions. A layer of material of the first conductivity type is provided on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions. The top layer of material and the substrate are subject to application of a reverse-bias voltage. None of the cited references show such structure.

Colak, U.S. Patent No. 4,626,879, shows a DMOS transistor suitable for source follower applications. This device has a substrate with three epitaxial layers formed thereon. A surface-adjoining channel region is diffused into the epitaxial layers and a source region is diffused into the channel diffusion above the channel region. A drain region is diffused into the top epitaxial layer. An extended drain

region is formed from a portion of the top epitaxial layer between the drain region and the channel region. The top and bottom epitaxial layers are interconnected, and the bottom layer may operate as a parallel extended drain region between the connection points. The intermediate epitaxial layer may operate as an extended drain region in a dual-gate/dual-drain structure wherein all three epitaxial layers contribute to device conductivity for achieving optimum normalized "ON" resistance.

Thomas, U.S. Patent No. 4,628,341 shows an integrated circuit structure that includes both low-voltage n-channel and p-channel MOS transistors and high voltage n-channel and p-channel MOS transistors.

The claims are now clearly distinguished from the cited references. New claim 19 recites "an extended drain region of the second conductivity type extending laterally each way from the drain contact pocket to surface-adjoining positions, a layer of material of the first conductivity type on top of an intermediate portion of the extended drain region between the drain contact pocket and the surface-adjoining positions". When high voltage n-channel and p-channel devices are combined on the same chip with low voltage control logic, this structure isolates the devices from each other. Claim 19 also provides for a pair of laterally spaced source and drain contact pockets within the substrate as is customary for conventional MOS transistors and is thus, distinguished from DMOS devices which require a higher threshold voltage. The structure of claim 19 enables a lower threshold voltage, compatibility with five volt control logic, and eliminates the need for an additional power supply and interface circuit.

Claims 20-22 and claims 6-7 depend directly or indirectly from claim 19 and thus, can be distinguished for the same reasons as claim 19.

Claim 23 is directed to the transistor, shown in Fig. 5 of the drawings, that has been modified for source-follower applications by providing both extended source and drain regions. Top layers cover intermediate portions of the extended source and drain regions. The top layers and substrate are subject to application of a reverse-bias voltage.

Accordingly, claims 6-7 and 20-23 are patentably distinct from the cited references and allowance of these claims is requested.

If the Examiner is of the opinion that a telephone conference with applicant's attorney would expedite matters, such a conference is invited.

Respectfully submitted,

Reg. No. 22,611

By _____
Thomas E. Schatzel

LAW OFFICES OF THOMAS E. SCHATZEL
A Professional Corporation
3211 Scott Boulevard, Suite 201
Santa Clara, California 95054
Telephone: (408) 727-7077

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on 4-7-88
(Date of Deposit)

Thomas E. Schatzel
Name of applicant, assignee, or Registered Rep.

_____ 4/7/88
Signature Date

Serial No.: 07/041,994
Filed: 4-24-87
Attnys. Docket No.: SS-520-01

PATENT

CONDITIONAL PETITION FOR EXTENSION OF TIME

If any extension of time for this response is required applicant requests that this be considered a petition therefor.

Status

This application is on behalf of:

___ other than a small entity

____ verified statement attached

__x__ small entity

__x__ verified statement already filed

Payment of fees

__X__ The Commissioner is hereby authorized to charge any additional fees as set forth in 37 C.F.R. 1.16 and 1.17 which may be required or credit any overpayment to Account No. 19-0310. A duplicate of this transmittal is attached.

NOTE: Please ____also
__X__ do not charge issues fees under 37 C.F.R. 1.18 to Account No. 19-0310.

Reg. No. 22,611

Attorney for Applicant

Telephone: (408) 727-7077

Law Offices of Thomas E. Schatzel
A Professional Corporation
3211 Scott Boulevard, Suite 201
Santa Clara, California 95054

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Thomas E. Schatzel
Name of applicant, assignee, or Registered Rep.

Signature 4/7/88 Date

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address : COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
07/041,994	04/24/87	EKLUND K	SS-520-01

THOMAS E. SCHATZEL
3211 SCOTT BLVD., STE. 201
SANTA CLARA, CA 95054-3093

EXAMINER	
JACKSON JR, J	
ART UNIT	PAPER NUMBER
253	4

DATE MAILED: 06/17/88

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☒ Responsive to communication filed on 4/11/88 ☒ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), ____ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice re Patent Drawing, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449
4. ☐ Notice of Informal Patent Application, Form PTO-152
5. ☐ Information on How to Effect Drawing Changes, PTO-1474
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☒ Claims 6, 7, 19-23 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 6, 7, 19-23 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings which are acceptable for examination purposes until such time as allowable subject matter is indicated.
8. ☐ Allowable subject matter having been indicated, formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. These drawings are ☐ acceptable; ☐ not acceptable (see explanation).
10. ☐ The ☐ proposed drawing correction and/or the ☐ proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved. ☐ disapproved (see explanation). However, the Patent and Trademark Office no longer makes drawing changes. It is now applicant's responsibility to ensure that the drawings are corrected. Corrections MUST be effected in accordance with the instructions set forth on the attached letter "INFORMATION ON HOW TO EFFECT DRAWING CHANGES", PTO-1474.
12. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

PTOL-326 (Rev. 7-82) EXAMINER'S ACTION

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless-

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 19, 6, 7 are rejected under 35 U.S.C. 102 (e) as anticipated by or, in the alternative, under 35 U.S.C. 103 as obvious over Colak.

Claim 19 still does not distinguish over Colak. See figures 1, 2B and 2C of Colak where 22 and 24 define "pockets", layers 18 and 14 form an "extended drain" which extends to the surface "each way" from the drain contact 24, layer 16 defines a layer of material of first conductivity type "on top of" extended drain layer 14, and layer 16 and substrate 12 are subject to application of a reverse bias voltage during operation of the device. Note that layer 16 is connected to the source and the substrate is reverse biased through SS. Thus claim 19 does not distinguish over Colak. Claim 5 is undistinguishing since Colak teaches a layer 16 thickness of 2 micron for 400 V operation, however, for lower voltage operation design layer 16 would be thinner, and 1 micron thickness is thus an obvious design variant to the artist. Similarly, to the artist, the design of claim 7 is obvious in view of Colak who teaches $10^{16}/cm^3$ for layer 16.

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Claims 20-23 are rejected under 35 U.S.C. 103 as being unpatentable over Colak in view of Thomas.

As stated in the previous rejection, Thomas shows that high voltage fet devices (as Colak) are advantageously formed complementary and also integrated with low voltage devices. Hence claims 20-22 are obvious.

Claim 23 is rejected under 35 U.S.C. 103 as being unpatentable over Sze.

Colak teaches punch through and avalanche protection layer 16 for a DMOS device. To one of ordinary skill it would have been obvious to practice the teachings of Colak in other MOS devices as ordinary fets as shown in Sze. Note figures 3, 51 or 52 of Sze where the source or drain are structurally similar and their function is dependent on the particular voltage applied. Hence, to the artist it would be obvious to apply the

teachings of Colak to symmetrical ordinary fets as shown in Sze to provide higher voltage operation.

Applicant's arguments filed April 11, 1988 have been fully considered but they are not deemed to be persuasive.

Applicant's argument that Colak does not show a drain "extending laterally each way" from the drain is not convincing as shown in the above rejection.

Clearly there is drain material 18 on each side of pocket 24.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, THIS ACTION IS MADE FINAL. See MPEP 706.07(a).

Applicant is reminded of the extension of time policy set forth in 37 CFR 1.136(a). The practice of automatically extending the shortened statutory period an additional month upon the filing of a timely first response to a final rejection has been discontinued by the Office. See 1021 TMOG 35.

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 CFR 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. Jackson whose telephone number is (703) 557-4824.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 557-3311.

J. Jackson:klw

6-15-88

(703) 557-4824

ANDREW J. JAMES
SUPERVISORY PATENT EXAMINER
GROUP ART UNIT 253

TO SEPARATE, HEED TOP AND BOTTOM EDGES, SNAP–APART AND DISCARD CARBON

FORM PTO-892 (REV. 3-78) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

NOTICE OF REFERENCES CITED

SERIAL NO.	GROUP ART UNIT	ATTACHMENT TO PAPER NUMBER
041994	253	4

APPLICANT(S): Eklund

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	A						
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						
	J						
	K						

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG	PERTINENT PP. SPEC.
	L								
	M								
	N								
	O								
	P								
	Q								

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

R	Sze, Physics of Semiconductor Devices Wiley & Sons N.Y. ©1981 pp 431-438, 486-491 (14) (14)
S	
T	
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EXAMINER	DATE
J. Jackson	6/88

* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05 (a).)